ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a plurality of memory cells, a memory cell array, bit lines, word lines, select gate lines, a column decoder, a first row decoder, a second row decoder, and first metal wiring. The memory cell includes a first MOS transistor with a charge accumulation layer and a control gate and a second MOS transistor connected to the first MOS transistor. The memory cell array has the memory cells arranged in a matrix. The word line connects commonly the control gates in the same row. The select gate line connects commonly the gates of the second MOS transistors in the same row. The first metal wiring layers are provided for every select gate lines, and pass through almost the central part of the memory cells. The first metal wiring layer is connected electrically to one of the select gate lines.